

**||Jai Sri Gurudev||**
  
**B.G.S INSTITUTE OF TECHNOLOGY**  
 B.G.Nagara-571448  
**Department of Electronics & Communication Engineering.**  
**III SEMESTER TIME TABLE FOR THE YEAR 2017-18**  
**For the period: Aug-Nov-2017**

Semester: III  
Section: A

Class Room: TB-02

Days	9:30-10:25AM	10:25-11:20AM	11:20-12:15AM	12:15-1:10PM	L U N C H  B R E A K	2:00-2:55 PM	2:55-3:50 PM	3:50-4:45 PM
Monday	15 EC 35	15 EC 36	15 EC 34	15 EC 33		HR TRAINING		
Tuesday	15 MAT 31	15 EC 34	15 EC 32	15 EC 33		15 EC 35	15 EC 34	15 MAT 31
Wednesday	15 EC 35	AEC Lab (A1) / DE Lab (A2)				15 MAT 31	15 EC 32	15 EC 36
Thursday	15 EC 36	15 EC 33	15 EC 32	15 MAT 31		15 EC 35	15 EC 33	15 EC 34
Friday	15 EC 36	15 EC 35	15 MAT 31	15 EC 32		AEC Lab (A2) / DE Lab (A1)		
Saturday	15 EC 32	15 EC 36	15 EC 33	15 EC 34				

Subject Code

Subject Name

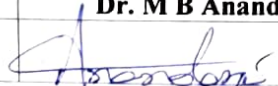

Staff Name

15 MAT 31  
15 EC 32  
15 EC 33  
15 EC 34  
15 EC 35  
15 EC 36  
15 ECL 37  
15 ECL 38

Engg. Mathematics-III  
Analog Electronics  
Digital Electronics  
Network Analysis  
Electronic Instrumentation  
Engineering Electromagnetics  
Analog Electronics Lab  
Digital Electronics Lab

Shwetha H N  
Kokila K S  
Kavitha B C  
Raghavendra L R  
Srividya C N  
Dr. Manjunatha R C  
Raghavendra L R  
Nandini S



Prepared by:	Dr. M B Anandaraju	Approved by:	Dr. B K Narendra
Signature		Signature	

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**III SEMESTER TIME TABLE FOR THE YEAR 2017-18**

For the period: Aug-Nov-2017

Semester: III

Section: B

Class Room: TB-03

Days	9:30-10:25AM	10:25-11:20AM	11:20-12:15PM	12:15-1:10PM	L U N C H  B R E A K	2:00-2:55 PM	2:55-3:50 PM	3:50-4:45 PM
Monday	15 MAT 31	15 EC 36	15 EC 33	15 EC 32		AEC Lab (B1) / DE Lab (B2)		
Tuesday	15 EC 35	15 EC 33	15 EC 34	15 EC 36		HR TRAINING		
Wednesday	15 EC 32	15 EC 36	15 MAT 31	15 EC 35		AEC Lab (B2) / DE Lab (B1)		
Thursday	15 EC 32	15 MAT 31	15 EC 34	15 EC 36		15 EC 34	15 EC 33	15 EC 35
Friday	15 EC 34	15 EC 32	15 EC 33	15 EC 35		15 MAT 31	15 EC 36	15 MAT 31
Saturday	15 EC 33	15 EC 34	15 EC 32	15 EC 35				

Subject Code

Subject Name

Staff Name

15 MAT 31  
 15 EC 32  
 15 EC 33  
 15 EC 34  
 15 EC 35  
 15 EC 36  
 15 ECL 37  
 15 ECL 38

Engg. Mathematics-III  
 Analog Electronics  
 Digital Electronics  
 Network Analysis  
 Electronic Instrumentation  
 Engineering Electromagnetics  
 Analog Electronics Lab  
 Digital Electronics Lab

Shwetha H N / Rashmi B T  
 Kokila K S  
 Nandini S  
 Puneeth Kumar G B  
 Srividya C N  
 Prabhavathi K  
 Dr. M B Anandaraju /Kavitha B C  
 Puneeth Kumar G B



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**III SEMESTER TIME TABLE FOR THE YEAR 2017-18**

For the period: Aug-Nov-2017

Semester: III  
 Section: C

Class Room: CR-13

Days	9:30-10:25AM	10:25-11:20AM	11:20-12:15AM	12:15-1:10PM	L U N C H  B R E A K	2:00-2:55 PM	2:55-3:50 PM	3:50-4:45 PM
Monday	15 EC 33	15 EC 32	15 EC 34	15 EC 36		15 EC 33	15 MAT 31	15 EC 35
Tuesday	15 EC 34	15 EC 36	HR TRAINING			AEC Lab (C1) /DE Lab (C2)		
Wednesday	15 EC 34	15 EC 32	15 MAT 31	15 EC 35		15 EC 36	15 EC 33	
Thursday	15 MAT 31	15 EC 36	15 EC 33	15 EC 32		AEC Lab (C2) /DE Lab (C1)		
Friday	15 EC 35	15 EC 32	15 EC 36	15 EC 34		15 EC 35	15 EC 32	15 MAT 31
Saturday	15 EC 35	15 MAT 31	15 EC 33	15 EC 34				

**Subject Code**

**Subject Name**

**Staff Name**

15 MAT 31  
 15 EC 32  
 15 EC 33  
 15 EC 34  
 15 EC 35  
 15 EC 36  
 15 ECL 37  
 15 ECL 38

Engg. Mathematics-III  
 Analog Electronics  
 Digital Electronics  
 Network Analysis  
 Electronic Instrumentation  
 Engineering Electromagnetics  
 Analog Electronics Lab  
 Digital Electronics Lab

Yuvaraja B K  
 Kavitha B C  
 Nandini S  
 Puneeth Kumar G B  
 Prafulla P S  
 Prabhavathi K  
 Kokila K S  
 Prabhavathi K



<b>Prepared by:</b>	<b>Dr. M B Anandaraju</b>	<b>Approved by:</b>	<b>Dr. B K Narendra</b>
Signature		Signature	



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**V SEMESTER TIME TABLE FOR THE YEAR 2017-18**

**For the period: Aug-Nov-2017**

Semester: V  
Section: A

Class Room: TB-05

Days	9:30-10:25AM	10:25-11:20AM	11:20-12:15AM	12:15-1:10PM	L U N C H  B R E A K	2:00-2:55 PM	2:55-3:50 PM	3:50-4:45 PM
Monday	15 EC 54	15 EC 562	15 ES 51	15 EC 53		DSP Lab (A1) / HDL Lab (A2)		
Tuesday	HR Training		15 EC 54	15 EC 562		15 EC 53	15 EC 52	15 EC 553
Wednesday	15 ES 51	15 EC 562	15 EC 553	15 EC 52		DSP Lab (A3) / HDL Lab (A1)		
Thursday	15 EC 53	DSP Lab (A2) / HDL Lab (A3)				15 EC 553	15 EC 54	15 ES 51
Friday	15 EC 52	15 EC 562	15 EC 553	15 EC 53		15 ES 51	15 EC 54	15 EC 52
Saturday	15 EC 562	15 EC 53	15 EC 52	15 EC 54				

**Subject Code**

**Subject Name**

**Staff Name**

15 ES 51

Management and Entrepreneurship

Balaji B S

15 EC 52

Digital Signal Processing

Anusha M N

15 EC 53

Verilog HDL

Shalini K J

15 EC 54

Information Theory & Coding

Jayanth Dwijesh H P

15 EC 553

Operating System

Prashanth N C

15 EC 562

Oops Using C++

Manoj Kumar S B

15 ECL 57

DSP Lab

Anusha M N

15 ECL 58

HDL Lab

Sri Vidya C N



<b>Prepared by:</b>	<b>Dr. M B Anandaraju</b>	<b>Approved by:</b>	<b>Dr. B K Narendra</b>
<b>Signature</b>		<b>Signature</b>	

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**V SEMESTER TIME TABLE FOR THE YEAR 2017-18**

**For the period: Aug-Nov-2017**

Semester: V  
 Section: B

Class Room: TB-04

Days	9:30-10:25AM	10:25-11:20AM	11:20-12:15AM	12:15-1:10PM	L U N C H  B R E A K	2:00-2:55 PM	2:55-3:50 PM	3:50-4:45 PM
Monday	HR Training		15 EC 52	15 EC 54		15 EC 53	15 EC 562	15 EC 553
Tuesday	15 ES 51	15 EC 562	15 EC 53	15 EC 52		DSP Lab (B1) / HDL Lab (B2)		
Wednesday	15 EC 53	15 EC 52	15 ES 51	15 ES 54		15 EC 553	15 EC 562	15 EC 53
Thursday	15 EC 562	15 ES 51	15 EC 553	15 EC 54		DSP Lab (B2) / HDL Lab (B3)		
Friday	15 EC 53	15 EC 54	15 EC 52	15 EC 562		DSP Lab (B3) / HDL Lab (B1)		
Saturday	15 EC 52	15 EC 54	15 EC 553	15 ES 51				

**Subject Code**

**Subject Name**

**Staff Name**

15 ES 51  
 15 EC 52  
 15 EC 53  
 15 EC 54  
 15 EC 553  
 15 EC 562  
 15 ECL 57  
 15 ECL 58

Management and Entrepreneurship  
 Digital Signal Processing  
 Verilog HDL  
 Information Theory & Coding  
 Operating System  
 Oops Using C++  
 DSP Lab  
 HDL Lab

Balaji B S  
 Anusha M N  
 Shalini K J  
 Jayanth Dwijesh H P  
 Prashanth N C  
 Manoj Kumar S B  
 Mohan Kumar K S  
 Manoj Kumar S B



<b>Prepared by:</b>	<b>Dr. M B Anandaraju</b>	<b>Approved by:</b>	<b>Dr. B K Narendra</b>
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**VII SEMESTER TIME TABLE FOR THE YEAR 2017-18**

For the period: **Aug-Nov-2017**

Semester: VII  
 Section: A

Class Room: TB-

Days	9:30-10:25AM	10:25-11:20AM	11:20-12:15AM	12:15-1:10PM	L U N C H	2:00-2:55 PM	2:55-3:50 PM	3:50-4:45 PM
Monday	10 EC 74	10 EC 73	10 EC 762	10 EC 72		B R E A K	VLSI (A1) / PE Lab (A3)	
Tuesday	10 EC 73	10 EC 72	10 EC 762	10 EC 751	VLSI (A2) / PE Lab (A1)			
Wednesday	10 EC 73	10 EC 74	10 EC 751	10 EC 71	VLSI (A3) / PE Lab (A2)			
Thursday	10 EC 762	10 EC 751	10 EC 73	10 EC 71		10 EC 74	10 EC 72	10 EC 751
Friday	10 EC 74	10 EC 71	10 EC 73	10 EC 751		10 EC 762	10 EC 72	10 EC 71
Saturday	10 EC 762	10 EC 71	10 EC 74	10 EC 72				

**Subject Code**

**Subject Name**

**Staff Name**

10 EC71  
 10 EC 72  
 10 EC 73  
 10 EC 74  
 10 EC 751  
 10 EC 762  
 10 ECL 77  
 10 ECL 78

Computer Communication Network  
 Optical Fiber Communications  
 Power Electronics  
 Embedded System Design  
 DSP Algorithms and Architecture (Elective B)  
 Real Time Systems (Elective C)  
 VLSI Lab  
 Power Electronics Lab

Amar Narayan  
 Dr. Manjunatha R C  
 Nandeesh M  
 Priyanka R  
 Naveen K B  
 Sandeep S V  
 Balaji B S  
 Jayanth Dwijesh H P

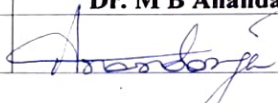
**Prepared by:**

**Dr. M B Anandaraju**

**Approved by:**

**Dr. B K Narendra**

**Signature**



**Signature**